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Amendments to the Specification:

AP 1/28/08 Please amend page 7, line ~~24~~ 23 as follows:

Figures 3, 4A, 4B, 4C, 4D, 4E, 5A, 5B, 6A, 6B, 7A1, 7A2, 7B, 8A, 8B, 9A, 9B, 10 illustrate different steps in the processes according to the invention for making a semiconductor device according to the invention.

AP 1/28/08 Please amend page 17, line ~~16~~ 13 as follows:

The metallic layer 51 forms the second metallisation area 51 (or cathode metallisation) that cooperates with the doped region 50 with the second type of conductivity (Figures 9A, 9B). Figure 9B illustrates the metallic deposit realized on the deice of figures 8A, 8B. Thus, the second metallisation area 51 is self-aligned with the first metallisation area 46, but without the need to use a complex lithography mask. The second metallisation area 51 is perfectly insulated electrically from the first metallisation area 46 by the dielectric layer 47.